The Stacked Capacitor DRAM Cell and Three-Dimensional Memory

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Device scaling and the DRAM cell

The key component in a computer system is memory, since both data and instructions in a stored-program-type computer are stored in main memory. Magnetic core memories, used in the early stages of computers, were replaced by semiconductor memories early in the 1970's. The first high density semiconductor memory was 1-Kbit dynamic random access memory (DRAM), developed by Intel. Since the advent of this 1-Kbit DRAM, the packing density and capacity of DRAM have continued to increase to today's 4Gbit. Such increases were achieved by the evolution of the memory cell from a four-transistor-type, three-transistor-type to a one-transistor- type. The invention of the one-transistor-type cell (1-T cell) by Robert Dennard especially accelerated the evolution of DRAM in conjunction with his device scaling theory [1, 2].

Scaling limitation of the planar (2D) DRAM cell

The one-transistor-type cell (1-T cell) consists of one transistor and one capacitor. A transistor acts as a switch, and the signal charges are stored in a capacitor. The first 1-T cell was realized using one switching transistor and one MOS capacitor. The number of signal charges stored in the storage capacitor has to be maintained at almost a constant, or can be only slightly reduced, as the memory cell size is scaled down. However, MOS capacitor value -- and hence the amount of signal charges – is significantly reduced as the memory cell size is reduced, even if the capacitor oxide thickness is scaled-down. Therefore, I forecast in 1975 that the 1-T cell with a two-dimensional (2D) structure using a planar MOS capacitor eventually would encounter a scaling-down limitation because we cannot reduce the MOS capacitor area according to scaling theory. In addition, I pointed out that the use of a MOS capacitor in the 1-T cell would be a problem because the signal charges are seriously reduced due to the influence of the minority carriers generated in a silicon substrate. An inversion layer capacitance and a depletion layer capacitance are connected with the gate oxide capacitance in parallel in the MOS capacitor. The charges in the inversion layer and the depletion layer are easily affected by the minority carriers, which are thermally or optically generated or generated by the irradiation of energetic particles in a silicon substrate. Therefore, I predicted that the 1-T cell using an MOS capacitor would encounter a scaling-down limitation due to the influence of the minority carriers as well.

Invention of the three-dimensional (3D) DRAM cell

In my Ph.D. research during 1971-1974 [3], I had commented on the silicon surface and the inversion layer in MOS structures. To evaluate the electrical properties of the interface states and the inversion layer, I myself built an impedance analyzer with the frequency range of 0.01Hz to 100MHz. I examined various kinds of capacitors, including high-k (high dielectric constant) capacitors as a reference capacitor of this impedance analyzer. Eventually, I made a vacuum capacitor for a reference capacitor in which fin-type capacitor electrodes were encapsulated in a vacuum container. From these studies, I learned that an ideal capacitor with low loss should consist of metal electrodes and a low loss insulator (MIM structure); a three-dimensional structure of capacitor electrodes is effective to increase the capacitance value, and there is a trade-off between high-k and loss in the capacitor insulator. In addition, I knew through my Ph.D. research that the charges in the inversion layer and the depletion layer are easily influenced by the minority carriers. Therefore, I questioned why the MOS capacitor with inversion capacitance and the depletion capacitance was used as the storage capacitor in the 1-T cell when I first knew about it in 1975. Then, I tried to eliminate the inversion capacitance and the depletion capacitance by employing a passive capacitor such as the MIM as a storage capacitor and thus proposed a three-dimensional (3D) cell in 1976 [4, 5]. I called this new 3D memory cell a stacked capacitor cell (STC).

Fabrication and evaluation of the three-dimensional stacked capacitor cell

Figure 1 shows the basic structure of a stacked capacitor cell (STC) where the storage capacitor is three-dimensionally stacked on a switching transistor [6, 7]. A passive capacitor with the structure of an electrode-

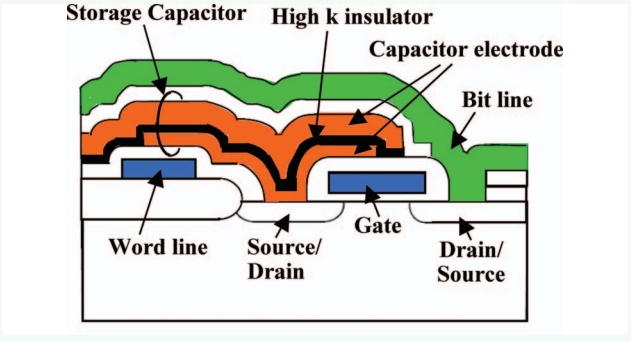

Fig. 1. Basic structure of stacked capacitor cell (STC).

insulator-electrode is used as a storage capacitor. The bottom electrode of the storage capacitor is connected to the source/drain region. I proposed to use self-aligned contacts to connect the bottom electrode of the storage capacitor and a bit line to the source/drain of the switching transistor. This self-aligned technique was also used for the formation of capacitor electrodes. By three-dimensionally stacking the storage capacitor on the switching transistor we can dramatically reduce the memory cell area. In addition, we can use a high-k material as a capacitor insulator to increase the storage capacitance, since a passive capacitor is used as a storage capacitor. This is also useful for reducing memory cell size. Furthermore, we can solve the problem that the signal charges in the inversion layer and depletion layer are influenced by the minority carriers since an inversion capacitance is not used in a stacked capacitor cell. In 1977, I fabricated the first DRAM test chip with a stacked capacitor cell using 3μm NMOS technology and presented a paper on the stacked capacitor cell in 1978 IEDM (IEEE International Electron Devices Meeting) [6]. Figure 2 shows the SEM cross section of a stacked capacitor cell fabricated using 3μm NMOS technology.

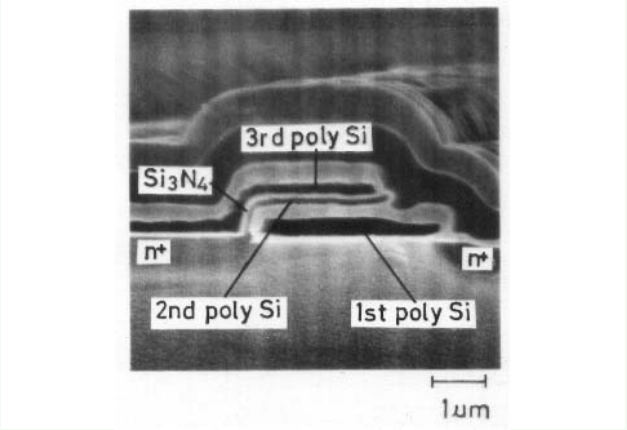

Fig. 2. SEM cross section of a stacked capacitor cell fabricated using 3um nMOS technology.

In this figure it is clearly shown that a storage capacitor is stacked on a switching transistor and a self-aligned contact is successfully formed, although plasma etching and RIE (reactive ion etching) were not available at the time. The self-aligned contact is widely used in today's memory LSI's. In this stacked capacitor cell, I employed polycrystalline silicon (poly-Si)- Si_3N_4 - polycrystalline silicon (poly-Si) as a storage capacitor. Thermal SiO_2 had been used as a capacitor insulator in a conventional 1-T cell with a MOS storage capacitor. In the stacked capacitor cell, I used Si_3N_4 instead of SiO_2 as a capacitor insulator to increase the storage capacitance. The dielectric constant of Si_3N_4 is approximately two times larger than that of SiO_2. I found that the leakage current of Si_3N_4 was significantly reduced by oxidizing its surface, as shown in Fig.3.

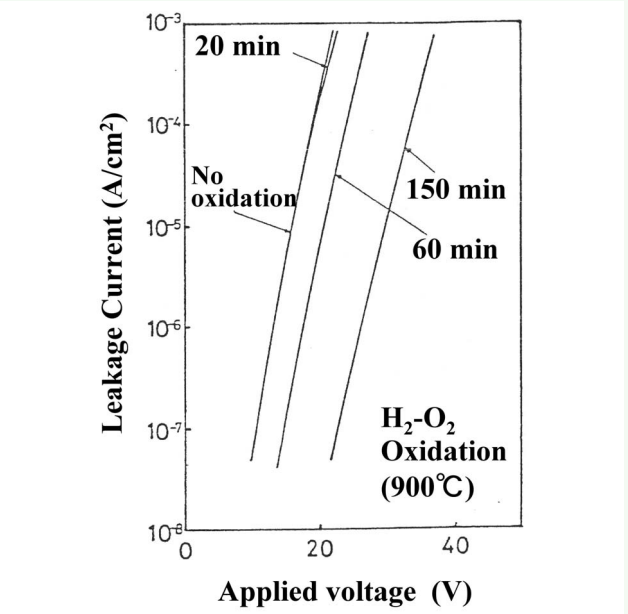

Fig. 3. Leakage-current versus applied-voltage characteristics for Si_3N_4 films with thin oxides on their surfaces.

I also used a Ta_2O_5 film as a capacitor insulator for the first time [7]. Ta_2O_5 has a dielectric constant five or six times larger than that of SiO_2. Therefore, we can greatly increase the storage capacitance, although the leakage current is larger compared to those of SiO_2 and Si_3N_4, as shown in Fig.4.

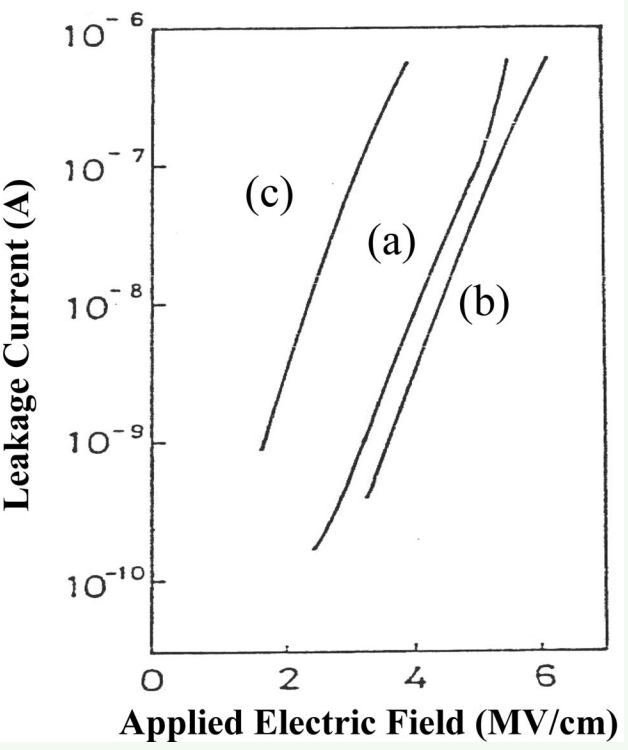

Fig. 4. Leakage current – applied electric field characteristics of storage capacitors. (a) poly-Si–SiO_2–poly-Si, (b) poly-Si–SiO_2 /Si_3N_4 (ON)–poly-Si, (c) poly-Si/Ta–Ta_2O_5–poly-Si.

In 1978, when I presented the first stacked capacitor cell paper in IEDM, it was revealed that the data retention characteristics of DRAM are seriously degraded due to "soft-error," which is caused by the carriers generated by alpha-particle irradiation in the silicon substrate. At that time, I believed that a stacked capacitor cell is tolerant of soft-error, since the signal charges stored in the passive capacitor are not influenced by the carriers generated in the substrate. Figure 5 shows the dependence of soft-error rate on cycle time in a DRAM test chip [8]. As I expected, the soft-error rate was dramatically reduced by employing a stacked capacitor cell.

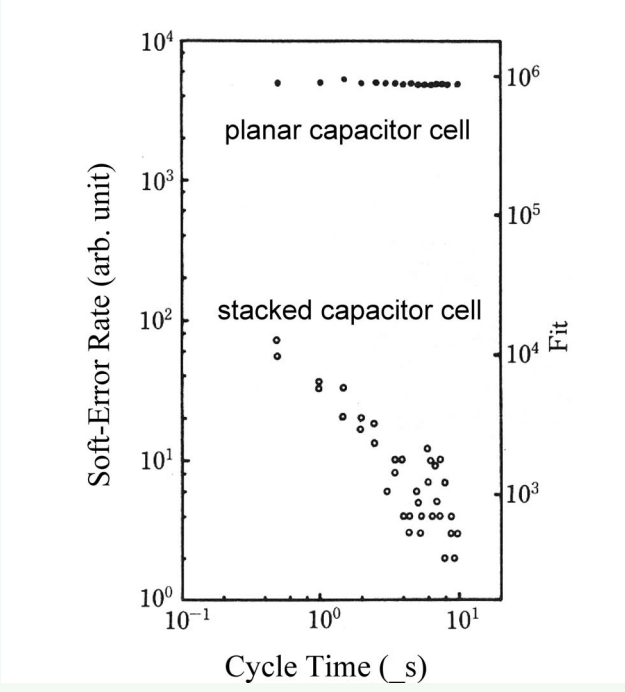

Fig. 5. Dependence of soft-error rate on cycle time in 16 K-bit DRAM test chip.

Eventually I proposed three types of stacked capacitor cells as shown in Fig.6 [9].

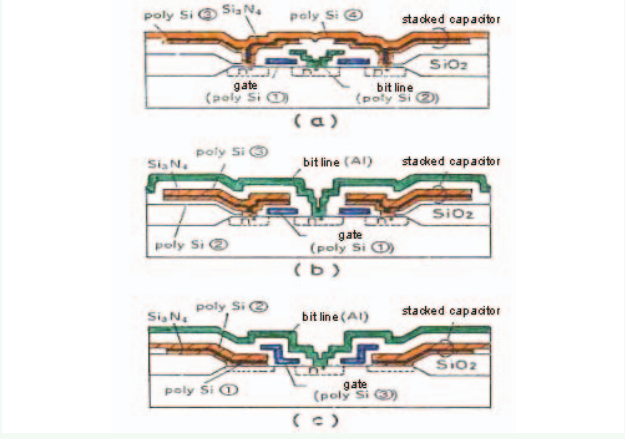

Fig. 6. Cross-sectional configuration of three types of stacked capacitor cells. (a) top-capacitor-type cell, (b) intermediate-capacitor-type cell, (c) bottom-capacitor-type cell.

A storage capacitor is stacked on the switching transistor and the bit line in a top-capacitor-type cell, on the switching transistor in the intermediate-capacitor-type cell (original stacked capacitor cell) and on the isolation oxide (LOCOS) in the bottom-capacitor-type cell. The top-capacitor-type STC cell is another name for the capacitor-over-bit line (COB) stacked capacitor cell and widely used in current DRAM [10]. We can use various kinds of materials for the capacitor insulator and electrodes, and can employ low temperature processes in the formation of the storage capacitor in the COB-type stacked capacitor cell since the storage capacitor is formed on the top of the memory cell.

Evolution of the three-dimensional (3D) memory cell and future memory

In 1979, I fabricated 16K-bit DRAM using a stacked capacitor cell with the oxidized Si_3N_4 (O/N) capacitor insulator [9]. Then I tried to introduce a stacked capacitor cell in 64K-bit DRAM production. However, it was too early to do this due to cost. As a result, the oxidized Si_3N_4 (O/N) capacitor insulator was employed in 64K-bit DRAM production. Since then, the oxidized Si_3N_4 (O/N) capacitor insulator has been widely used for DRAM production. A stacked capacitor cell was employed in a 1Mbit DRAM production for the first time by Fujitsu [11]. Hitachi also employed a stacked capacitor cell in 4Mbit DRAM production [12]. Many other DRAM companies used a trench capacitor cell in the early stage of 4Mbit DRAM production. However, the stacked capacitor cell, which eventually came to occupy a major position in 4Mbit to 4Gbit DRAM's, has evolved by introducing the three-dimensional capacitor structures with fin-type electrode [13] and cylindrical electrode [14] in conjunction with a capacitor electrode surface morphology of hemi-spherical grain (HSG) [15]. In addition to the introduction of the three-dimensional capacitor structure, a storage capacitor insulator with high dielectric constant (high-k) was employed in high density DRAM's. In general, the leakage current of high-k material increases by high temperature processing. Therefore, a COB-type stacked capacitor cell is suitable for introducing a high-k capacitor insulator since the storage capacitor can be formed by a lower temperature process. Thus, the Ta_2O_5 capacitor insulator was employed in 64Mbit and 256Mbit DRAM's with a COB-type stacked capacitor cell. Since then, various kinds of high-k materials have been studied as storage capacitor insulators in high density DRAM's beyond 1Gbit. The concept of the COB-type stacked capacitor cell -- that various kinds of materials can be stacked on the switching transistor using a lower temperature process -- has been carried on in new memories with a three-dimensional structure such as Fe-RAM (Ferroelectric RAM), P-RAM (Phase Change RAM), R-RAM (Resistive RAM) and M-RAM (Magnetic RAM).

In a high density stacked capacitor DRAM beyond 16 Gbit, a twitching transistor with a three-dimensional structure such as a Fin-FET and a vertical transistor

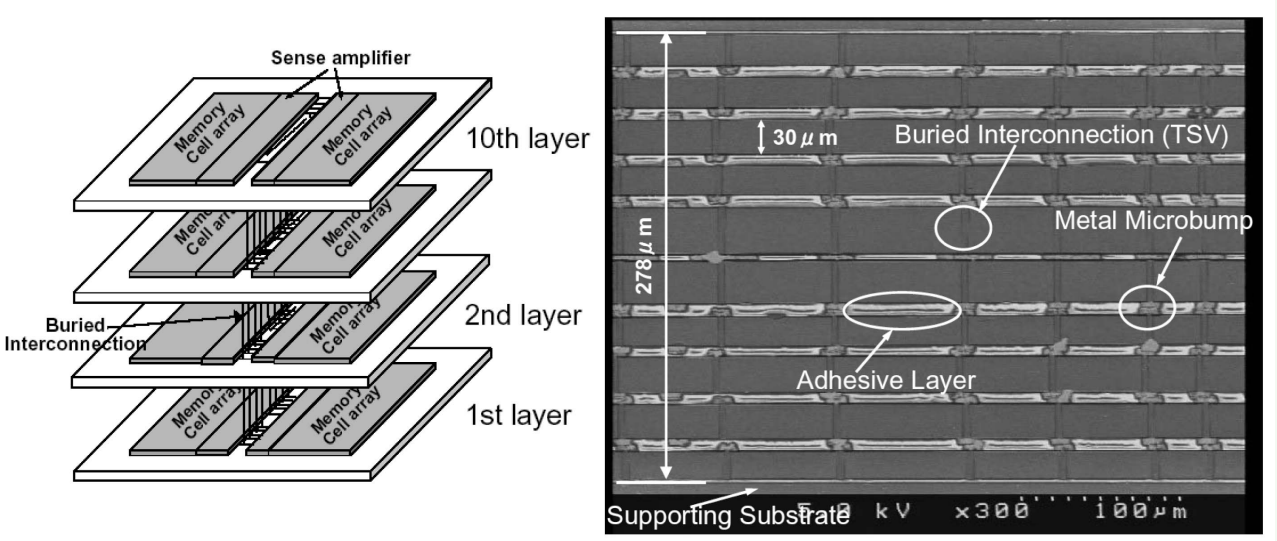

Fig. 7. SEM cross section of 3D-DRAM test chip with ten memory layers fabricated by wafer-on-wafer bonding technology with through-silicon-vias (TSV's).

will be employed together with a cylindrical capacitor and high-k capacitor insulator. Furthermore, many DRAM chips eventually will be vertically stacked to realize 3D-DRAM in which the memory capacity dramatically increases. We have already succeeded in fabricating a 3D-DRAM test chip with ten memory layers as shown in Fig.7 [16, 17].

This 3D-DRAM test chip was fabricated using a newly developed wafer-on-wafer bonding technology with through-silicon-vias (TSV's) [18-20]. Such a 3D-DRAM can be directly stacked on a microprocessor chip to realize a 3D-microprocessor and to solve the problems of memory data-bandwidth between the memory and the processor. We also fabricated a 3D-microprocessor test chip in which a DRAM chip is stacked on a processor chip, as shown in Fig.8 [21].

In the future, various kinds of LSI chips, sensor chips and MEMs chips will be vertically stacked into an ultimate 3D-LSI which we call a super-chip [17, 22]. We have developed a new super-chip integration technology using a novel self-assembly method.

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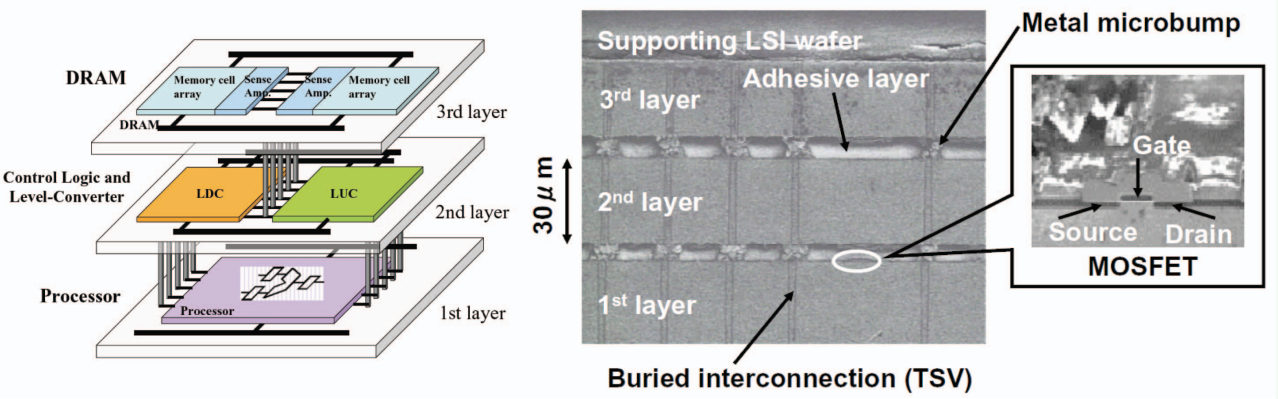

Fig. 8 SEM cross section of a 3D-microprocessor test chip fabricated by wafer-on-wafer bonding technology with through-silicon-vias (TSV's).

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About the Author

Mitsumasa Koyanagi was born in 1947 in Hokkaido, Japan. He received the B.S. degree from Department of Electrical Engineering, Muroran Institute of Technology, Japan in 1969 and the M.S. and Ph.D. degrees from Department of Electronic Engineering, Tohoku University in 1971 and 1974, respectively.

He joined the Central Research Laboratory, Hitachi Co. Ltd. in 1974 where he had engaged in the research and development of DRAM and ASIC process and device technologies and invented a Stacked Capacitor DRAM memory cell which has been widely used in DRAM production. In 1985, he joined Xerox Palo Alto Research Center, where he was responsible for research on submicron CMOS devices, poly-Si TFT devices and analog/digital sensor LSI design. In 1988, he became a professor in the Research Center for Integrated Systems, Hiroshima University, Japan where he engaged in the research of sub-0.1um device fabrication and characterization, device modeling, poly-Si TFT devices, 3-D integration technology, optical interconnection and parallel computer system. He proposed a 3-D integration technology based on wafer-to-wafer bonding and through-Si vias (TSVs) in 1989. Since 1994, he has been a professor in the Intelligent System Design Lab., Department of Machine Intelligence and Systems Engineering, and is currently a member of the Department of Bioengineering and Robotics, Graduate School of Engineering, Tohoku University, Japan. His current interests are 3-D integration technology, optical interconnection, nano-CMOS devices, memory devices, parallel computer system specific for scientific computation, real-time image processing system, artificial retina chip and retinal prosthesis chip, brain-machine interface (BMI) and neural prosthesis chip, brain-like computer system.

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